METHOD OF IMPROVED TDICCD DESIGN BASED ON SENSOR CLOCKING

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KEY WORDS: TDICCD, Taps Merging, Continuous Transfer Clocking, Pixel Binning, Area Array mode;

ABSTRACT:
The final output signal quality of TDICCD is related to the key parameters such as working mode, output mode, signal-to-noise ratio, dynamic range and so on. We can improve these parameters of TDICCD by reasonably designing the sensor clocking. Therefore, this text discussed four methods of improved TDICCD sensor clocking to solve some problem in TDICCD application based on using the principle of TDICCD. The technique of TDICCD Taps merging can reduce the number of TDICCD Taps, which helps to reduce the size of the TDICCD rear-end circuit significantly; The technique of TDICCD continuous transfer clocking can improve the charge transfer efficiency, which helps to promote the final signal-to-noise ratio; The technique of pixel binning clocking can enlarge the dynamic range of image; The technique of TDICCD area-array working mode can extend the field of TDICCD working; The principle, derivation process, clocking sequence diagram and application range of these clocking design schemes are given in this paper. At the same time, it also explains its actual effect and the matters to be noted.

1. INTRODUCTION

The high-precision long-line array time-delay integral charge-coupled device (TDICCD) is used for the satellite multispectral remote sensing camera. Because TDICCD is the initial source of remote sensing image data, the quality of its output signal plays a vital role in the whole imaging system. The TDICCD mode of operation, the charge transfer process and the quality of the TDICCD output signal are all directly related to the design of TDICCD sensor clocking. References respectively study the characteristics, noise status, application patterns and corresponding sensor clocking of TDICCD. TDICCD in practical applications of space remote sensing engineering, the following problems are often encountered :1) Most of the TDICCD used are long-line arrays, with up to 20 output signals, resulting in a very large image acquisition circuit. The weight, volume, power consumption and cost of the camera are multiplied ;2) TDICCD transfer clock will cross into the TDICCD output image analog signal, how to suppress this crosstalk noise? 3) Whether can we use timing technology to realize pixel merging in TDICCD analog signal source output to improve signal quality ;4) Since the basic structure of the TDICCD is an array CCD, can it perform array imaging besides linear array push scan imaging? On the basis of introducing the principle and structure of the TDICCD, this paper further improves the basic four-phase TDI timing by using the basic principle of TDICCD timing, and creatively puts forward four TDICCD timing design techniques, such as analog tap merging timing technology, TDICCD continuous transfer timing technology, pixel binning timing technology and TDICCD array imaging technology, which can solve the engineering problems mentioned above satisfactorily. Since the TDICCD sensor clocking design is processed at the source of the remote sensing image signal, it can simplify the imaging circuit conveniently and efficiently, improve the signal-to-noise ratio (SNR) of the image, the range of the sensor's dynamic response, and expand the TDICCD's working adaptation.

Time delay and integrating sensors (TDI) is a special application of area sensors for linear imaging. In this technique the linear image is mechanically scanned from the top to the bottom of the sensor. Functionally, it is a linear array device. The rows of the TDICCD are the levels of time delay and integrating, the columns of it are the number of pixels in a row of TDICCD. Based on multiple exposures to the same target, the photosensitive charge packet is integrated by delay to enhance the collection of light energy. It can easily solve the contradiction between sensitivity and speed and resolution.

Next, we use moving ball to simulate the process of ground pixel passing through the TDICCD array to further describe: (see figure 1)

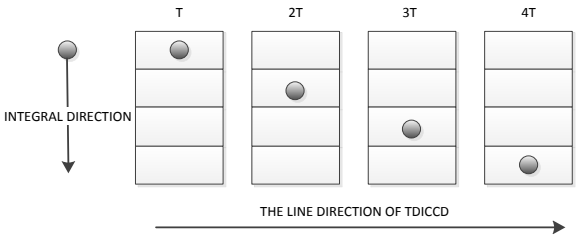

Figure 1. Principle of the TDICCD

In the process of scanning image along the direction of the TDICCD column, in the first integration period, the ball carries on the exposure integration in the first pixel of a column, and the photosensitive charge is not read out like the ordinary CCD, and then it moves down one pixel. In the second integration period, the ball happens to move to the second pixel of the column for exposure integration, and the resulting photosensitive charge is added with the charge moved from the previous pixel, and then moved to the next pixel. Until the NO.M integral period, the target has been moved to the NO.M pixel of the column for exposure integration, and the photosensitive charge of the No. M pixel is added to the sum of all previous pixels and moved into the readout register which is like an ordinary CCD device. It can be seen that the charge read out is M times that of a single pixel, while the noise only increases by $\sqrt{M}$ times. Therefore, the sensitivity of TDICCD is much better than that of ordinary CCD device.

Specifically, the theory of TDICCD is that the vertical CCD registers are clocked to ensure that the charge packets are transferred at the same rate and in the same direction as the image. This ensures that the signal charge building up in the CCD remains aligned under the same part of the image. In this way, the image signal can be integrated for much longer than is allowed by the temporary storage time of a single pixel. The sensitivity of the sensor is increased by a factor roughly equal to the number of “stages” in the vertical direction. Hence the TDI CCD sensor can be used in low light levels, or used at very high

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scan speeds. It has the further advantage of averaging out any nonuniformities in each vertical column and gives an enhanced signal to noise ratio.

2. THE STRUCTURE AND SENSOR CLOCKING PRINCIPLE OF TDICCD

For two dimensional images an area array is formed from a set of parallel light sensitive CCD registers, which by convention are assumed to be orientated up and down the page. At the lower edge of this array a single horizontal CCD register (HCCD) is used to combine the outputs from the vertical registers (VCCD) into a single output. Among them, the clock that drives the parallel linear array register to transfer vertically is CI1~CI4, the clock that drives the horizontal transfer register is CR1~CR4. At the bottom of the sensor a transfer gate clock (TCK, SCK) is often used to control the movement of charge into the horizontal readout register. Often an additional transfer gate is positioned between the horizontal register and the vertical CCD registers to prevent charge transfer into the horizontal register while it is being emptied. The control charge readout clock CRLST and RG is inserted at the end of the horizontal readout registers. When the CCD charge is finally readout, it is necessary to draw out n readout taps according to the actual readout rate. The basic structure of TDICCD is as shown in Figure 2.

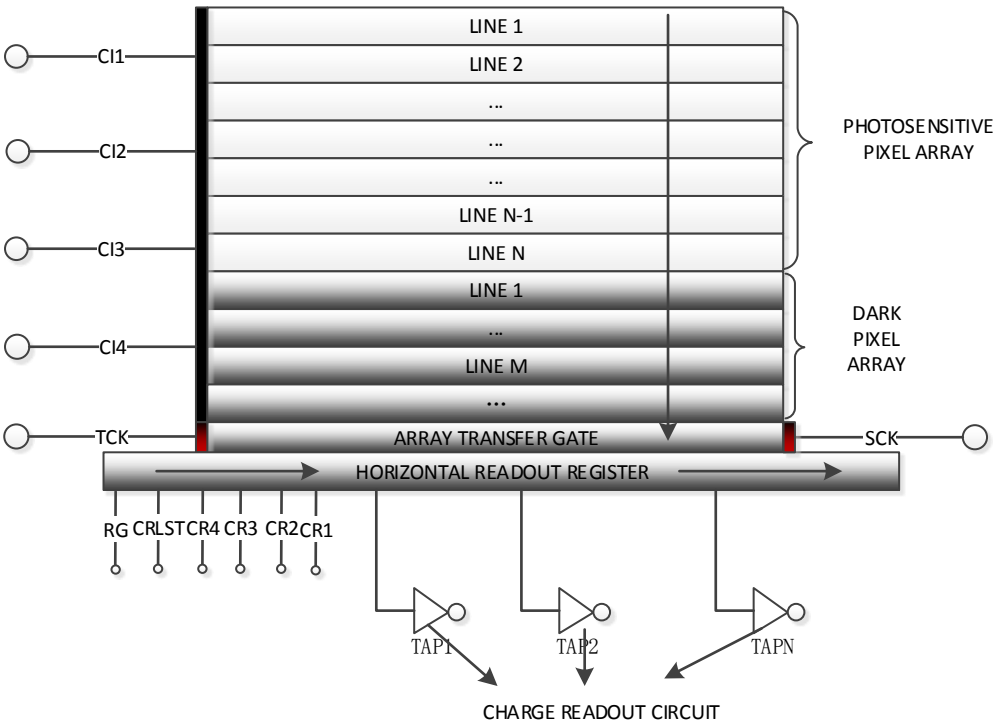

Figure 2. Sketch of TDICCD structure

A common clocking technique is the 4-phase clocking system which uses 4 gates per pixel. See Figure 3. At any given time, two gates act as barriers (no charge storage) and two provide charge storage. In normal operation the process begins when the right most storage gate is switched to a higher (positive) voltage. See Figure 4. This widens the storage region towards the righthand barrier and allows the charge to spread out underneath the extra storage gate. At the same time, the left most storage gate is switched to a lower voltage. This narrows the storage region from the lefthand side and forces the charge into the region underneath the remaining two storage gates. The net result is a movement of the signal charge to the right by one gate width. This clock sequence is repeated another three times to move the charge packet along to the next pixel. By clocking the gates continuously, it is possible to shift the charge along the register from left to right. In the horizontal CCD this process is called readout, and the readout clocks are designated CR1, CR2, CR3 and CR4. The transfer gate between the horizontal and vertical registers is controlled by the transfer clock TCK, the output capacitor reset clock is designated RST. In TDI sensors the transfer of charge down the vertical CCD registers is controlled by the imaging clocks CI1, CI2, CI3 and CI4. CCD uses a variety of clock sequence to complete the different transfer effects of photosensitive charges.

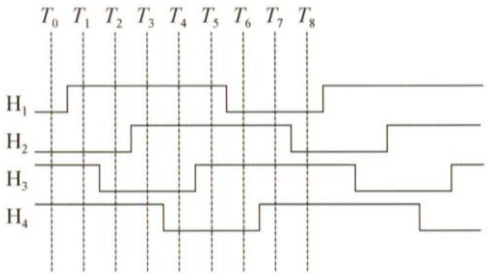

Figure 3. 4-phase clocking system

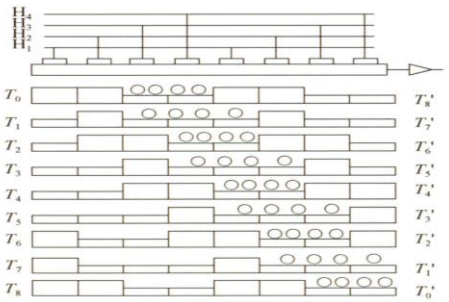

Figure 4. Charge motion driven by 4-phase clocking

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During the TDICCD, the sensor uses a variety of sensor clock-driven coordination to achieve different transport effect of photosensitive charge. Here are a few clocking design techniques, all by the sensor charge transfer clocking design, on the basis of common basic four-phase timing to improve the design, and finally can achieve such important functions as multi-tap merging, improve charge transfer efficiency, image element simulation merging and TDICCD surface array imaging. Smart timing design can improve image quality and expand the function of sensor.

3. TDICCD TAPS MERGING TECHNOLOGY

A Long Array of TDICCD usually has more than 10 taps. The quantization of each of these taps will use a lot of AD devices, and produce many quantized digital signals, which makes the circuit design area too large and it is difficult to receive data synchronization. We can realize the combination of multiple CCD analog taps by designing a tap to synthesize the clocking and cooperating with the analog switch. The following example is given to illustrate the merging of two analog taps into one analog tap.

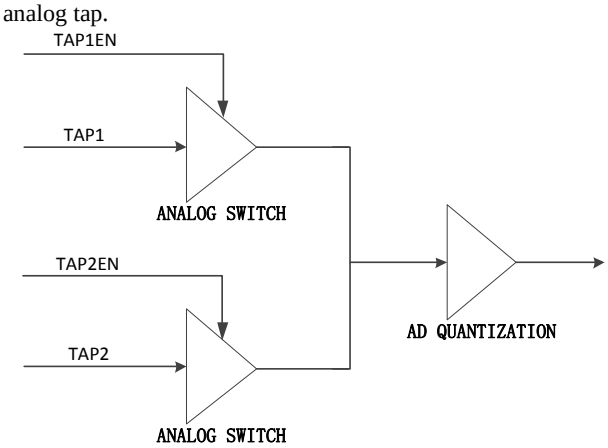

Figure 5. Schematic diagram of analog merging hardware

Fig.5 is the schematic diagram of analog merging hardware. In the figure 5, TAP1 and TAP2 are the analog taps of the CCD output, providing analog signal input to the analog switch. TAP1EN and TAP2EN are used as the enable signals of the analog switch to control the on and off of the analog signal. After the output signals of the two analog switches are directly connected, the AD is sent to quantize and output a road of digital signal.

The design of the TDICCD clocking signal matched with figure 5 is shown in figure 6: CIXs are the vertical transfer clocks of TDICCD, which complete the vertical transfer of normal TDICCD charge, and its period is equal to the row transfer period of TDICCD. The horizontal transfer clocking signals that control TDICCD charge readout of each tap are designed separately. Stagger the horizontal transfer clocking of TAP1 and the horizontal transfer clocking of TAP2 in order to fully ensure their time mutual exclusion. That is, when Tap1 is transferred, TAP2 does not transfer, and vice versa.

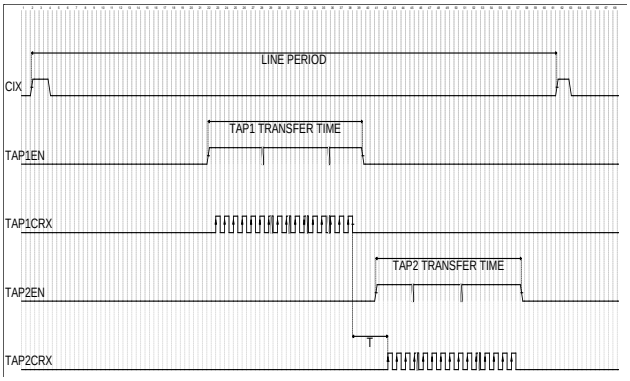

Figure 6. Analog merging clock sequence diagram

When designing the sensor clocking, we should pay attention to the following points: firstly, the CRX signal is bound to the TAPXEN signal in groups and the high level of TAPXEN covers all CRX signals. Secondly, there is a safe time interval T between one signal group and another signal group to ensure that the analog switch has enough time to complete the switching from one signal to another. Finally, different signal groups are generated by the same clock, which is a fully synchronous signal, so it is convenient for the back-end AD to sample at the same clock frequency.

The schematic diagram of the merged analog signal of TDICCD output is shown in figure 7.

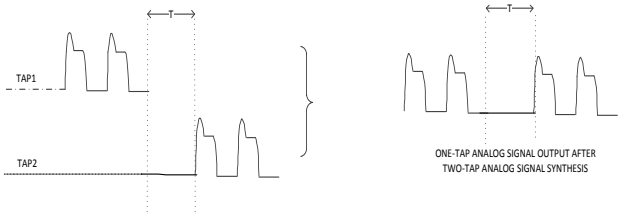

Figure 7. Result picture after analog merging

As can be seen from the above picture, through the strict fully synchronous sensor clocking design, the analog signals output by the two taps of TDICCD can be merged into on analog signal. This technology can greatly reduce the volume and power consumption of sensor circuits under the premise of sufficient data bandwidth.

4. TDICCD CONTINUOUS TRANSFER CLOCKING TECHNOLOGY

During readout of the horizontal CCD it is possible to continue transfer of the image using CI1-CI4 in preparation for a quick transfer into the horizontal register when the transfer clock goes high. However, this can result in feedthrough of the CI clock edges into the video signal. This feedthrough can be avoided using burst mode clocking, whereby the CI clocks are held fixed until the horizontal CCD has been read out. Unless the speed penalty is unacceptable this scheme is recommended. As a result, TDICCD continuous transfer clock technology is introduced to solve this problem.

The photosensitive zone VCCD (CI) clocks are planned to be operated in a continuous manner and not in burst mode. This feature helps in improving the vertical MTF of the device. In addition to the slow CI clocks, each zone has an independent fast storage clock (SCK) for the fast transfer of charge from the VCCD into the horizontal shift register. The continuous transfer clocks as shown in Figure 8. The active time of TCK or SCK only accounts for a small part of the whole line period. The horizontal

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shift clock is not allowed during this time, but outside this time, the CR clock can be sent continuously. In this way, the continuity of CI and CR clock is ensured as much as possible, thus the MTF value of CCD is improved and the circuit noise caused by burst mode is reduced.

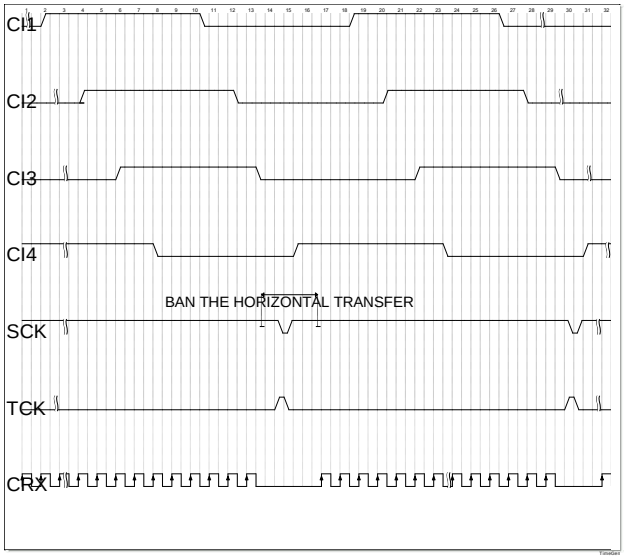

Figure 8. Continuous transfer clock sequence diagram

TDICCD continuous transfer clocking technology maximizes the isolation of vertical transfer clocking and horizontal transfer clocking by controlling the clocking design of electrode SCK and TCK between vertical and horizontal transfer of sensors, so that the clocking of horizontal transfer is not related to the timing of vertical transfer. Then CI clocking can be designed as a continuous clock with a duty cycle of 50% and also extends the transmission time of the CRX timing. Thus, the TDICCD charge transfer efficiency (CTE) is improved and the resulting transfer crosstalk noise is reduced; on the other hand, the time of horizontal transfer is also increased, which also extends the TDICCD output data rate bandwidth.

5. TDICCD BINNING

A special clocking arrangement can be used to combine charge packets from a number of neighboring pixels before sending them to the output amplifier. This reduces the spatial resolution of the sensor, but provides an improved signal-noise ratio in low light conditions by combining several small charge packets. As with the TDI sensor, the addition of many charge packets reduces the noise level by averaging out pixel to pixel variations. This technique is referred to as pixel binning.

Binning in TDICCDs is a readout technique that allows the user to change sensor resolution dynamically by applying a special clock sequence to the sensor. This Technique combines several charge packets from adjacent pixels into a single charge packet thus effectively increasing pixel size (forming a so-called “superpixel”). For example, binning with factor of 2 in both vertical and horizontal directions. (also called 2X2 binning) for a nXn micron pixel CCD sensor is equivalent to a 2nX2n micron pixel CCD sensor with same overall imager size, but with 4 times less total number of pixels. Note that binning in vertical and in horizontal directions can be performed independently.

To implement binning in the horizontal direction, charge is binned either in the readout node directly or under the last HCCD gate which will have an independent control (usually labelled as CRLAST). In order to achieve binning factor of N, only one RST(and CRLAST) clock is applied for N CRX clocks. The waveform of CRLAST is shown in the following figure 9.

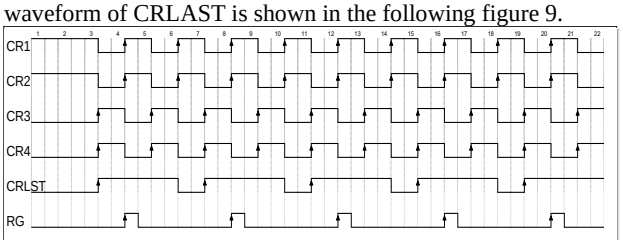

Figure 9. Horizontal binning clock sequence Diagram

For vertical binning, several parallel line transfers occur in a row while the HCCD is in steady-state conditions (receiving charge packets from the image section). Charge packets from individual pixels are summed up in HCCD elements directly. Again, for a binning factor of N, N vertical transfer clocks (N CIX period) must be applied during a single line transfer time（one SCK or TCK period).

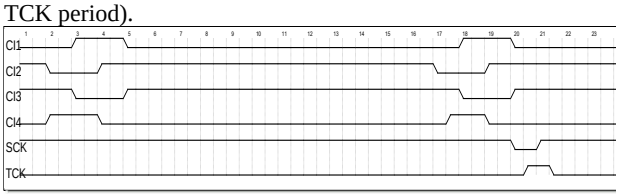

Figure 10. Vertical Binning clock sequence diagram

Relative to the digital method, TDICCD binning technique improves the dynamic range of the image and the signal-to-noise ratio of the output signal while completing the downsampling of the image. Therefore, it greatly improves the quality of the output signal and low-light imaging ability of the TDICCD camera.

6. TDICCD AREA ARRAY IMAGING TECHNOLOGY

According to the structure of TDICCD (see figure 2), TDICCD is essentially an area ccd with M columns and N rows. In the time delay integration mode, with the same integration time period, N pixels in the same column are exposed to the same target, and the final accumulated charge is read out together. In the process of imaging, it is necessary to ensure that the image transfer velocity of TDICCD matches the charge transfer speed exactly. If you want to use TDICCD to obtain area array image, the TDICCD must be static during exposure. At this time, the image transfer speed is 0, and the charge transfer speed does not match the image transfer speed. If the integration time period is long enough relative to the charge transfer time, the image blurring caused by TDICCD charge transfer can be ignored, that is, the area array imaging of TDICCD camera is realized.

E_{N1}	E_{N2}	·····	E_{NM}
$E_{(N-1)1}$	$E_{(N-1)2}$	·····	$E_{(N-1)M}$
⋮	⋮	⋮	⋮
E_{11}	E_{12}	·····	E_{1M}

Figure 11. TDICCD photosensitive charge distribution

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Suppose that in a row transfer period T, the photosensitive charge generated by each pixel of TDICCD is shown in Figure 11, that is, the photosensitive charge generated by row i and column j pixel is E_{ij} . Assume the integration time

$$T_{int} = kT(k > 1) \qquad (1)$$

According to the principle of TDICCD, it is known that the time for all n-line images to be transferred is NT. Since the TDICCD is still integrating during the charge transfer period, the photosensitive charge generated by the pixel of row i and column j during the whole integration time and charge transfer time is

$$E_t = kE_{ij} + \sum_{i=i}^{N-1} E_{ij} \qquad (2)$$

. It can be seen from the formula that the equivalent charge of the output image consists of two parts, one is the photosensitive charge kE_{ij} generated by the TDICCD pixel during the integration time, and the other photosensitive charge during the vertical transfer of pixel is $\sum_{i=i}^{N-1} E_{ij}$. If $kE_{ij} >> \sum_{i=i}^{N-1} E_{ij}$, that is to say, the photosensitive charge generated by TDICCD pixel in the integration time is much larger than that during the vertical transfer of the TDICCD pixel. It can be known that the vertical transfer charge in the final total charge can be ignored, and the total charge output of the image pixel is

$$E_t \cong kE_{ij} \qquad (3)$$

.the area array mode output of TDICCD is realized.

According to the formula T_{int}=kT(Equation 1), the condition can be satisfied if k is greater than 1000. The TDICCD clock sequence diagram is shown in Figure 12. It can be seen from the figure that when the frame period is fixed, the time of the clock sequence action is much less than the time when it is at rest.

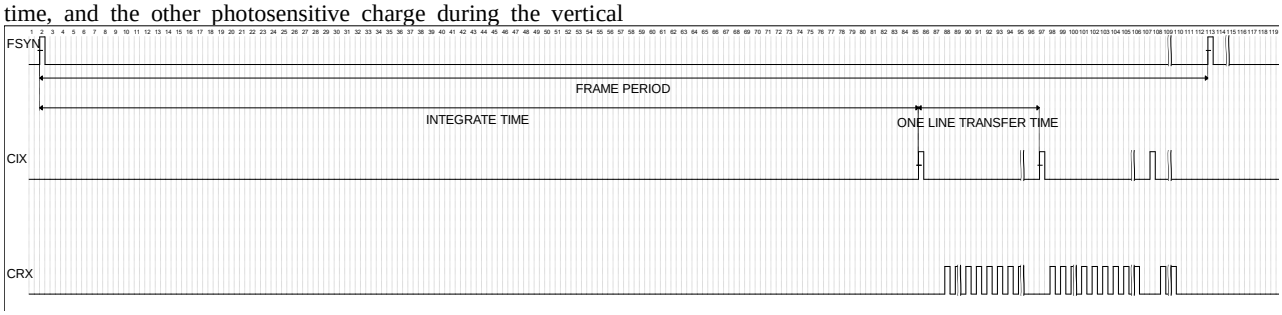

Figure 12. TDICCD area array imaging clock sequence diagram

TDICCD area array imaging technology extends its application field, which make it can image not only in linear scan mode for Objects moving synchronously but also in area array mode for a static object. This brings great flexibility, for example, the same TDICCD camera can image the Earth and the Sun in different working mode.

7. CONCLUSION

In this paper, it introduces TDICCD structure and sensor clocking principle, and then discusses four methods of TDICCD clocking, which combined with the problems in the practical application of TDICCD camera. These techniques can reduce the number of TDICCD analog taps, improve TDICCD charge transfer efficiency, pixel dynamic response range and readout signal-to noise ratio. Moreover, the linear array working mode of TDICCD is extended to the area array application mode which brings great flexibility to TDICCD applications. The clocking control of TDICCD has great plasticity. We can apply the principle of TDICCD charge transfer to improve the clock sequence in order to solve some practical problems in TDICCD application engineering.

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